Confirmation no. 9391 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	LETAVIC	Examiner:	Hu, Shouxiang
Serial No.:	10/574,065	Group Art Unit:	2811
Filed:	March 30, 2006	Docket No.:	US030375US2 (NXPS.493PA)
Title:	LATERAL THIN-FILM SOI DEVICE HAVING A FIELD PLATE WITH ISOLAED METALLIC REGIONS		

APPEAL BRIEF

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Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed November 30, 2009 and in response to the rejections of claims 1-18 as set forth in the Final Office Action dated September 2, 2009.

Please charge Deposit Account number 50-4019 (US030375US2) $540.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 019719/0843 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-18 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments to the claims have been filed subsequent to the Final Office Action dated September 2, 2009. An amendment to the specification was filed with the response to the Final Office Action; however this amendment was not entered by the Examiner.

V. Summary of Claimed Subject Matter

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject

matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

Commensurate with independent claim 1, an example embodiment of the present invention is directed to a lateral thin-film Silicon-On-Insulator (SOI) device (*see, e.g.*, transistor 20 shown in Figs. 1 and 2) comprising: a semiconductor substrate (*see, e.g.*, substrate 22 shown in Fig. 1 and page 3:12-22), a buried insulating layer on said substrate (*see, e.g.*, buried insulating layer 24 shown in Fig. 1 and page 3:12-22), and a lateral MOS transistor device in an SOI layer on said buried insulating layer (*see, e.g.*, SOI layer 26 shown in Fig. 1 and page 3:12-22) and having a source region of a first type conductivity (*see, e.g.*, source region 28 shown in Fig. 1 and page 3:12-22) formed in a body region of a second type conductivity (*see, e.g.*, body region 30 shown in Fig. 1 and page 3:12-22), a lateral drift region of a second type conductivity adjacent said body region (*see, e.g.*, lateral drift region 32 shown in Fig. 1 and page 3:12-22), a drain region of said first type conductivity and laterally spaced apart from said body region (*see, e.g.*, drain region 34 shown in Fig. 1 and page 3:12-22), a gate electrode insulated from said body region and drift region by an insulation region (*see, e.g.*, gate electrode 36 shown in Fig. 1 and page 3:12-22), an insulation layer on and laterally adjacent to the gate electrode (*see, e.g.*, insulation region 38 shown in Fig. 1 and page 3:12-22), and a field plate on the insulation layer and separated from the gate electrode and the drain extension region by the insulation layer (*see, e.g.*, field plate 52 shown in Fig. 1 and page 3:23 to page 4:13), the field plate being connected either to said source region or said gate electrode and extending substantially over said lateral drift region (*see, e.g.*, region 52a shown in Fig. 1 and page 4:1-13), wherein said field plate comprises a first layer of plural metallic regions which are isolated laterally from one another so as to form a linear lateral electric field distribution in the lateral drift region (*see, e.g.*, regions 52a and 52b shown in Fig. 1 and page 4:1-13).

Commensurate with independent claim 13, an example embodiment of the present invention is directed to a lateral thin-film Silicon-On-Insulator (SOI) device (*see, e.g.*, transistor 20 shown in Figs. 1 and 2) comprising: a semiconductor substrate (*see, e.g.*, substrate 22 shown in Fig. 1 and page 3:12-22); a buried insulating layer on the substrate (*see, e.g.*, buried insulating layer 24 shown in Fig. 1 and page 3:12-22); and a lateral MOS transistor device in an SOI layer on said buried insulating layer (*see, e.g.*, SOI layer

26 shown in Fig. 1 and page 3:12-22) and having a source region of a first conductivity type (*see, e.g.*, source region 28 shown in Fig. 1 and page 3:12-22) formed in a body region of a second conductivity type (*see, e.g.*, body region 30 shown in Fig. 1 and page 3:12-22), a lateral drift region of the second conductivity type adjacent the body region (*see, e.g.*, lateral drift region 32 shown in Fig. 1 and page 3:12-22), a drain region of the first conductivity type and laterally spaced apart from the body region by the lateral drift region (*see, e.g.*, drain region 34 shown in Fig. 1 and page 3:12-22), a gate electrode insulated from said body region and drift region by an insulation region (*see, e.g.*, gate electrode 36 shown in Fig. 1 and page 3:12-22), an insulation layer on and laterally adjacent to the gate electrode (*see, e.g.*, insulation region 38 shown in Fig. 1 and page 3:12-22), source and drain contact regions in a layer region including the gate electrode and respectively electrically contacting the source and drain regions, the contact regions being laterally separated from the gate electrode by the insulation layer (*see, e.g.*, source contact electrode 42 and drain contact electrode 44 shown in Fig. 1 and page 3:23 to page 4:13), and a field plate arrangement, on the insulation layer, having a plurality of conductive regions that laterally extend substantially over the lateral drift region and that are insulated from one another by an insulative material (*see, e.g.*, field plate 52 shown in Fig. 1 and page 3:23 to page 4:13), a first one of the conductive regions at a first end of the field plate being connected either to the source region or the gate electrode (*see, e.g.*, region 52a shown in Fig. 1 and page 4:1-13), the conductive regions linearly distributing a voltage at the first conductive region across the other conductive regions to an opposite end of the field plate, the distributed voltage dropping laterally across the field plate from the first end to the opposite end (*see, e.g.*, regions 52a and 52b shown in Fig. 1 and page 4:1-13).

VI. Grounds of Rejection to be Reviewed Upon Appeal

The grounds of rejection to be reviewed on appeal are as follows:

A. Claims 1-18 stand rejected under 35 U.S.C. § 112(1).

B. Claims 5 and 17 stand rejected under 35 U.S.C. § 112(2).

C. Claims 1-18 stand rejected under 35 U.S.C. § 103(a) over Letavic (U.S. Patent No. 6,127,703) in view of Nakagawa (U.S. Patent No. 4,614,959).

D. An objection to the drawings.

VII. Argument

A. The § 112(1) Rejections Of Claims 1-18 Are Improper Because The Identified Aspects Are Supported By Appellant's Disclosure, The Rejections Are Based On Language That Is Not Present In The Claims, And The Rejections Are Based On An Erroneous Conclusion By The Examiner.

1. The Rejection Of Claims 1 and 13 Is Improper Because Claim Aspects Directed To The Field Plate Being Connected To The Gate Electrode Are Supported By Appellant's Disclosure.

Claims 1 and 13 are fully supported by Appellant's disclosure in compliance with the written description requirement. The rejection is predicated on a misapplication of the written description requirement and the Examiner has improperly maintained the rejection despite the fact that Appellant has specifically indentified portions of Appellant's specification that provide support for the aspects of the claims asserted to be the basis for these rejections. In particular, the indentified aspects of claim 1 (*e.g.*, the field plate being connected to the gate electrode) are original claim limitations for which the Examiner has never established "why persons skilled in the art would not recognize in the disclosure a description of the invention defined by the claims." *See, e.g.*, M.P.E.P. § 2163 ("There is a strong presumption that an adequate written description of the claimed invention is present when the application is filed.").

More specifically, Appellant has at least twice provided the Examiner with a detailed explanation regarding support for claim aspects directed to the field plate being connected to the gate electrode. For example, paragraph 0021 of the published version of the instant application recites "the field plate 32 may be an extension, or connected to, the gate electrode 36 instead of the source region 42." The figures and the incorporated references further assist in an understanding of such an embodiment, with a multitude of connection options readily apparent to one of skill in the art. Moreover, amended FIG. 1 shows dashed lines with item number 37, as one exemplary manner in which to form such a connection. As such, the above discussed aspects of claims 1 and 13 are fully supported in compliance with the written description requirement. Appellant respectfully

submits that the Examiner's apparent confusion regarding "how the gate electrode and the field plate could be connected together" does not rebut the clear support in Appellant's disclosure for the field plate being connected to the gate electrode. Appellant notes that claims 1 and 13 do not specify how the gate electrode and the field plate are connected together and, as such, the Examiner has not presented any basis for a rejection under the written description requirement. The field plate and the gate electrode can be connected in any number of manners as would be readily apparent to the skilled artisan based on Appellant's disclosure, as discussed above.

In view of the above, the § 112(1) rejection of claims 1 and 13 is improper and Appellant requests that it be reversed.

2. The Rejection Of Claim 11 Is Improper Because Claim Aspects Directed To The Capacitive Coupling Of The Metallic Regions Of The Field Plate And The Related Linear Voltage Distribution Across The Field Plate Are Supported By Appellant's Disclosure.

Aspects of claim 11 directed to a first one of the metallic regions in the field plate being connected to the source region and the remaining ones of the metallic regions being capacitively coupled to the first one of the metallic regions to linearly distribute a voltage at the source region across the field plate are fully supported by Appellant's disclosure in compliance with the written description requirement. The Examiner has improperly maintained the rejection despite the fact that Appellant has specifically indentified portions of Appellant's specification that provide support for such aspects of the claimed invention. *See, e.g.*, M.P.E.P. § 2163.

More specifically, support for these aspects can be found throughout Appellant's disclosure including, for example, in Appellant's Figure 1 which shows field plate segment 52a connected to source region 42 and segments 52b being isolated from segment 52a. Paragraph 0016 of the published version of the instant application further states that

> Because of the isolation, unlike in the prior art where the voltage throughout the whole field plate is the same as the high voltage +Vs of the source region, the voltage in the field plate of the present invention is linearly distributed laterally. In other words, it drops linearly from the same high voltage +Vs of the source region 42 at its most left region (i.e., the region 52a) to a much lower value at the end of the field plate 52, i.e., at its most right region.

As such, the above discussed aspects of claim 11 are fully supported in compliance with the written description requirement. Appellant respectfully submits that the Examiner's apparent confusion regarding "how the voltage at the source region across the field plate could be linearly distributed" does not rebut the clear support in Appellant's disclosure for such aspects as discussed above. Appellant notes that the Examiner further discusses the gate electrode being on the path between the source region and the field plate, however, such aspects are not recited in claim 11 and, as such, do not form any basis for a rejection under the written description requirement.

In view of the above, the § 112(1) rejection of claim 11 is improper and Appellant requests that it be reversed.

3. The Rejection Of Claims 1 And 14 Is Improper Because Claim Aspects Directed To A Linear Lateral Electric Field Distribution In The Lateral Drift Region Are Supported By Appellant's Disclosure.

Claims 1 and 14 are supported by Appellant's disclosure in compliance with the written description requirements. The Examiner erroneously asserts that aspects directed to the field plate including a first layer of plural metallic regions which are isolated laterally from one another so as to form a linear lateral electric field distribution in the lateral drift region are not supported by Appellant's disclosure. Appellant submits that support for such aspects can be found throughout Appellant's disclosure including, for example, in paragraph 0016 of the published version of the instant application which discusses that there is a linear voltage distribution across the metallic regions 52a and 52b of the field plate. Paragraph 0018 of the published version of the instant application further states that

> The lateral drift region 32 is preferably provided with a linearly-graded charge profile over at least a major portion of its lateral extent such that the doping level in the lateral drift region 32 increases in a direction from the drain region 34 toward the source region 28. In such a situation, the field plate preferably has a lateral electric field distribution or profile that exactly follows the electric field in the SOI drift region 32.

As another example, as initially discussed in the Abstract of the instant application and as consistent with the description of the figures, example embodiments of the present invention are directed to a device that generates a lateral electric field profile using "a volume doping gradient in the silicon drift region." The resulting electric field (*e.g.*, in

the structure 32 as shown in FIG. 1) is thus not only influenced by the distribution of voltage across the field plate, it is further influenced by the arrangement and composition of the doping gradient in the device. As further discussed at paragraph 0004 of the published version of the instant application, prior approaches to applying an electric field explicitly teach away from the claimed invention, and involve determining the electric field with a "capacitive field plate chain" in which the "doping in the drift region does not determine the lateral electric field." The Examiner's unsupported conclusion that the resulting electric field "must be nonlinear" (see page 4 of the final Office Action) thus contradicts the claimed invention and Appellant's specification. Accordingly, the above discussed aspects of claims 1 and 14 are fully supported by Appellant's disclosure in compliance with the written description requirement.

Moreover, the Examiner's further assertions regarding the claimed invention being inconsistent with an empirical relationship between an electrical field and voltage distribution do not form any basis for a rejection under the written description requirement. In particular, the Examiner's assertions are not based on Appellant's disclosure being inconsistent with the claimed subject matter, which is clearly supported as discussed above.

In view of the above, the § 112(1) rejection of claims 1 and 14 is improper and Appellant requests that it be reversed.

4. The Rejection Of Claims 1 And 14 Is Improper Because The Claims Do Not Recite That The Voltage And The Electrical Field Are Both Linear In The Same Region.

The sole basis for the rejection of claims 1 and 14 is the Examiner's assertion regarding an empirical relationship between an electrical field and voltage distribution and the Examiner's conclusion that the "the voltage (or potential) and the field cannot both be simultaneously linear in any region" (page 4 of the final Office Action). The claimed invention, however, does not recite that the voltage and the electrical field are both simultaneously linear in a given region. For example, claim 1 recites a linear lateral electric field distribution in the lateral drift region, without mentioning the voltage distribution in the lateral drift region and without making any reference to the voltage or electric field distributions in any other region. As another example, claim 14 recites a linear lateral electric field distribution in the lateral drift region without mentioning the

voltage distribution the lateral drift region and claim 14 recites a linear voltage distribution across the field plate without mentioning the electric field distribution in the field plate. As such, the Examiner's assertions are not based on Appellant's claim language. Accordingly, the Examiner's assertions do not form any basis for a rejection under the written description requirement.

In view of the above, the § 112(1) rejection of claims 1 and 14 is improper and Appellant requests that it be reversed.

5. The Rejection Of Claims 1 And 14 Is Improper Because The Rejection Is Based On The Examiner's Erroneous Assertion That A Constant Electrical Field Is Not Linear.

Appellant submits that a constant electric field is linear and, as such, the Examiner has failed to present any basis for the rejection of these claims. In particular, the Examiner appears to recognize that a constant electric field is linear in stating that "a linear distribution is not always constant" (page 4 of the final Office Action). Appellant agrees with the Examiner that a linear distribution is not always constant; however, since a linear distribution can be constant, the Examiner's assertion that a constant electrical field is not linear is clearly erroneous.

In view of the above, the § 112(1) rejection of claims 1 and 14 is improper and Appellant requests that it be reversed.

6. The Rejection Of Claims 17 And 18 Is Improper Because Claim Aspects Directed To The Lateral Drift Region Having A Doping Gradient That Generates A Linear Lateral Electric Field Distribution Are Supported By Appellant's Disclosure.

Aspects of claims 17 and 18 directed to the lateral drift region including dopants arranged with a doping gradient that generates, in response to a voltage applied to the field plate arrangement, a linear lateral electric field distribution in the lateral drift region are fully supported by Appellant's disclosure in compliance with the written description requirement. The Examiner has improperly maintained the rejection despite the fact that Appellant has specifically indentified portions of Appellant's specification that provide support for such aspects of the claimed invention. *See, e.g.*, M.P.E.P. § 2163.

More specifically, support for these aspects can be found throughout Appellant's disclosure including, for example, in paragraphs 0016 and 0018 of the published version

of the instant application which discuss that the electric field profile in the field plate exactly follows the electric field profile in drift region 32 and that it is "the linearly-graded charge profile" in the lateral drift region 32 that causes such a relationship. Thus, there is a linear lateral electric field distribution in the drift region 32, as is discussed in further detail above in connection with claims 1 and 14. The Examiner has failed to provide any rebuttal to Appellant's explanation with regard to support for the indentified aspects of claims 17 and 18 as required, for example, by M.P.E.P. § 2163.

In view of the above, the § 112(1) rejection of claims 17 and 18 is improper and Appellant requests that it be reversed.

B. The § 112(2) Rejection Of Claims 5 And 17 Is Improper Because The Examiner Has Improperly Equated The Breadth Of The Claims With Indefiniteness.

Claims 5 and 17 do particularly point out and distinctly claim the subject matter which Appellant regards as the invention. In this instance, the Examiner has improperly equated breadth of the claims with indefiniteness. *See, e.g.,* M.P.E.P. § 2173.04 ("Breadth of a claim is not to be equated with indefiniteness."). The purported basis for the rejection of claim 5 is that claim 5 fails to clarify the relationship of the term "another dielectric layer" to the "insulation layer" of claim 1. Appellant notes that § 112(2) and applicable law does not require that the term "another dielectric layer" necessarily bear any specific relationship with the insulation layer recited in claim 1. Regarding claim 17, the Examiner asserts that claim 17 fails "to clarify what is the feature that is definitely responsible for the generation of the recited linear field in the drift region." Once again, § 112(2) and applicable law does not require that Appellant identify such a feature. However, Appellant notes that claim 17 does recite that the lateral drift region includes dopants arranged with a dopant gradient that generates the linear electric field distribution. Accordingly, the Examiner has improperly equated breadth with indefiniteness.

In view of the above, the § 112(2) rejection of claims 5 and 17 is improper and Appellant requests that it be reversed.

C. The § 103(a) Rejection Of Claims 1-18 Is Improper Because The Cited References Fail To Disclose A Field Plate That Linearly Distributes Voltage.

The Examiner has not established correspondence to all claim limitations, including those directed to a field plate that linearly distributes voltage, or to a device that operates with a field plate (and related structure) that generates a linear electric field distribution in a lateral drift region. Generally, the Examiner's assertion that the electric field in the underlying drift region of the cited references "would have a lateral distribution that would be naturally substantially same as whatever the distribution is in the instant invention" is untenable (*see* page 8 of the Final Office Action). Nothing of record suggests that the cited drift region 32 of the '703 reference exhibits a linear electric field distribution.

More specifically, regarding the § 103 rejection of independent claim 13 and as applicable to the rejections of all claims, the Examiner has failed to show how the cited plate regions 6', 13' and 7' of the '959 reference would linearly distribute voltage when implemented in the '703 reference or otherwise. On the contrary, it appears that the plate layer 6' is at least four times wider than both of the plate layers 13' and further that the plate layer 7' has a width that is between the width of the plate 6' and plates 13'. Accordingly, it does not appear to be possible that the cited field plate layers of the '959 reference could linearly distribute voltage as claimed because the plate regions of different sizes would respectively effect voltage across varying lengths of underlying regions (*e.g.* the voltage drop would appear to be "stepped" relative to the varying lengths of the plate regions). As such, the Examiner's assertions of inherency with regard to the voltage distribution across the plate in the '959 reference are improper. *See, e.g.,* M.P.E.P. § 2112 ("Inherency, however, may not be established by probabilities or possibilities."). Thus, the Examiner has provided no explanation whatsoever as to how the voltage could be distributed as claimed. This is also consistent with the description of the claimed invention, which describes the use of plates spaced at specific intervals to achieve the claimed linear voltage distribution (*see, e.g.*, paragraphs 0019 and 0020 of the published version of the instant application). Accordingly, nothing of record suggests that the structure of the '959 reference as combined with the '703 reference would operate as in the claimed invention.

In view of the above, the § 103 rejections are improper because they have failed to establish correspondence to all claim limitations, including those directed to generating a linearly-distributed electric field (*e.g.*, independent claim 1) and to a field plate having a linear voltage distribution (*e.g.*, as in independent claims 1 and 13). Accordingly, Appellant requests that the § 103 rejections of claims 1-18 be reversed.

D. The Objection To The Drawings Is Improper Because The Drawings Do Show The Features Of The Claims That Are Essential For A Proper Understanding Of The Claimed Invention.

The objection to the drawings is improper because the objection relies upon an improper interpretation of the U.S.P.T.O. rules. Specifically, the Examiner erroneously asserts that the drawings "must show every feature of the invention specified in the claims." The definition of a feature is a prominent attribute or aspect of something. Rather than limit the cited rule to prominent aspects of the claims, the Office Action appears to take the position that the figures must provide a near word-for-word correspondence to the claims. The Examiner's position, if applied to all cases, would ostensibly require that every patent application contain a near word-for-word replication of all language from the claims into the figures. Moreover, Appellant's position is also supported by a number of U.S. laws, U.S.P.T.O. rules and passages of the M.P.E.P. This support is largely inconsistent with the Examiner's position and will be discussed hereafter.

The Examiner's apparent interpretation of 37 CFR § 1.83(a) is contrary to the U.S.P.T.O. practice, U.S. law and the M.P.E.P. In support of Appellant's position reference is made to 35 USC § 113, which indicates that an "applicant shall furnish a drawing where necessary for the understanding of the subject matter sought to be patented." *See also* M.P.E.P. § 601.01(f). The authority for the U.S.P.T.O. to create rules such as 37 C.F.R. § 1.83(a) is derived from 35 USC § 113. Accordingly, 37 C.F.R. § 1.83(a) must be interpreted in light of this law to ensure that the U.S.P.T.O. does not exceed the statutory authority granted by the U.S. Congress. Moreover, M.P.E.P. § 608.02(e) clarifies how 37 C.F.R. § 1.83(a) should be interpreted and applied by an examiner: "The drawings are objected to under 37 CFR 1.83(a) because they fail to show [1] as described in the specification. Any structural detail *that is essential for a proper understanding of the disclosed invention* should be shown in the drawing." (*emphasis*

added). This language is the suggested paragraph for an examiner that wishes to use a 37 C.F.R. § 1.83(a) objection. The Examiner conveniently has not used this language, choosing instead to ignore the second half of the suggested language.

Referring now to the claim language at issue, Appellant submits that support for the identified aspects can be found in Appellant's Figure 1 which shows a field plate (*e.g.*, portions 52a and 52b) on an insulation layer 38 with insulation layer 38 being above gate electrode 36 and the portion 52a is connected to the gate electrode by an exemplary connection shown by dashed lines 37. Thus, the drawings are sufficient to show the recited features in a manner that would provide one of skill in the art with a complete understanding of the invention. Appellant notes that Figures 1 and 2 are cross-sectional views of semiconductor devices and, as such, necessarily do not show all connections between every layer of the devices as would be readily understood by the skilled artisan and is common practice in the illustration of such devices.

In view of the above, the objection to the drawings is improper and Appellant requests that it be reversed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-18 are improper and therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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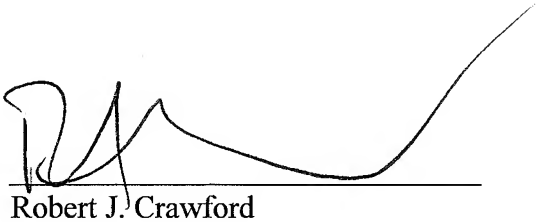
By: 

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/574,065)

1. A lateral thin-film Silicon-On-Insulator (SOI) device comprising

a semiconductor substrate,

a buried insulating layer on said substrate, and

a lateral MOS transistor device in an SOI layer on said buried insulating layer and having

a source region of a first type conductivity formed in a body region of a second type conductivity,

a lateral drift region of a second type conductivity adjacent said body region,

a drain region of said first type conductivity and laterally spaced apart from said body region,

a gate electrode insulated from said body region and drift region by an insulation region,

an insulation layer on and laterally adjacent to the gate electrode, and

a field plate on the insulation layer and separated from the gate electrode and the drain extension region by the insulation layer, the field plate being connected either to said source region or said gate electrode and extending substantially over said lateral drift region, wherein said field plate comprises a first layer of plural metallic regions which are isolated laterally from one another so as to form a linear lateral electric field distribution in the lateral drift region.

2. The device of claim 1 wherein said isolated metallic regions are located in a layer that is vertically above a layer including the gate electrode, and are isolated from one another by a dielectric layer.

3. The device of claim 2 wherein said field plate further comprises another layer of plural metallic regions located above said dielectric layer in spaces between the metallic regions, laterally isolated from one another, and isolated from said metallic regions of said first layer by said dielectric layer.

4. The device of claim 3 wherein said dielectric layer is a silicon-rich nitride layer.

5. The device of claim 4 further comprises another dielectric layer provided between said field plate and said MOS transistor device.

6. The device of claim 1 wherein said lateral drift region is provided with a linearly-graded charge profile.

7. The device of claim 6 wherein said linear lateral electric field distribution follows an electric field in said drift region.

8. The device of claim 7 wherein said first type conductivity is p-type conductivity, and said second type conductivity is n-type conductivity.

9. The device of claim 3 wherein said first type conductivity is p-type conductivity, and said second type conductivity is n-type conductivity.

10. The device of claim 1 wherein said first type conductivity is n-type conductivity, and said second type conductivity is p-type conductivity.

11. The device of claim 1 wherein a first one of said metallic regions in the field plate is connected to said source region and the remaining ones of said metallic regions are capacitively coupled to the first one of said metallic regions to linearly distribute a voltage at the source region across the field plate.

12. The device of claim 1 wherein a first one of said metallic regions in the field plate is connected to said gate electrode and the remaining ones of said metallic regions are capacitively coupled to the first one of said metallic regions to linearly distribute a voltage at the gate electrode across the field plate.

13. A lateral thin-film Silicon-On-Insulator (SOI) device comprising

a semiconductor substrate;

a buried insulating layer on the substrate; and

a lateral MOS transistor device in an SOI layer on said buried insulating layer and having

a source region of a first conductivity type formed in a body region of a second conductivity type,

a lateral drift region of the second conductivity type adjacent the body region,

a drain region of the first conductivity type and laterally spaced apart from the body region by the lateral drift region,

a gate electrode insulated from said body region and drift region by an insulation region,

an insulation layer on and laterally adjacent to the gate electrode,

source and drain contact regions in a layer region including the gate electrode and respectively electrically contacting the source and drain regions, the contact regions being laterally separated from the gate electrode by the insulation layer and

a field plate arrangement, on the insulation layer, having a plurality of conductive regions that laterally extend substantially over the lateral drift region and that are insulated from one another by an insulative material, a first one of the conductive regions at a first end of the field plate being connected either to the source region or the gate electrode, the conductive regions linearly distributing a voltage at the first conductive region across the other conductive regions to an opposite end of the field plate, the distributed voltage dropping laterally across the field plate from the first end to the opposite end.

14. The device of claim 13, wherein the field plate arrangement linearly distributes an electric field across the lateral drift region.

15. The device of claim 13, wherein the field plate arrangement provides a linearly-graded charge profile to the lateral drift region, the charge profile dropping linearly from a high charge profile below the first end of the field plate arrangement to a low charge profile below the opposite end of the field plate arrangement.

16. The device of claim 1, further including

a source contact region electrically coupled to the source region, having an extension above the gate on the insulation layer, and being separated both laterally and vertically from the gate electrode by the insulation layer, and

a drain contact region electrically coupled to the drain region, having an extension on the insulation layer, and being separated laterally from the gate electrode by the insulation layer,

the field plate extending between the extensions of the source contact region and the drain contact region on the insulation layer.

17. The device of claim 1, wherein the lateral drift region includes dopants arranged with a doping gradient that generates, in response to a voltage applied to the field plate, the linear lateral electric field distribution in the lateral drift region.

18. The device of claim 13, wherein the lateral drift region includes dopants arranged with a doping gradient that generates, in response to a voltage applied to the field plate arrangement, a linear lateral electric field distribution in the lateral drift region.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.